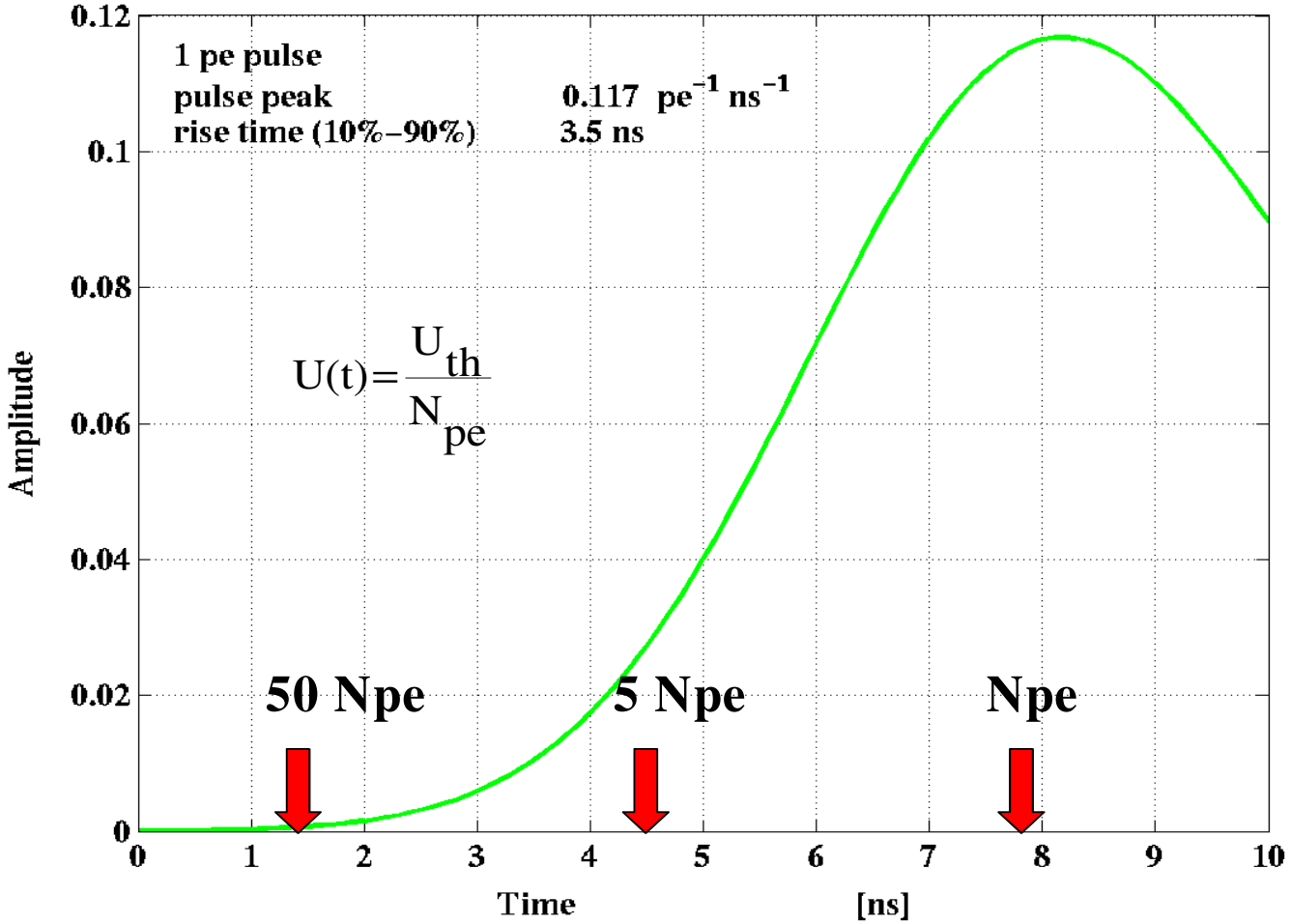
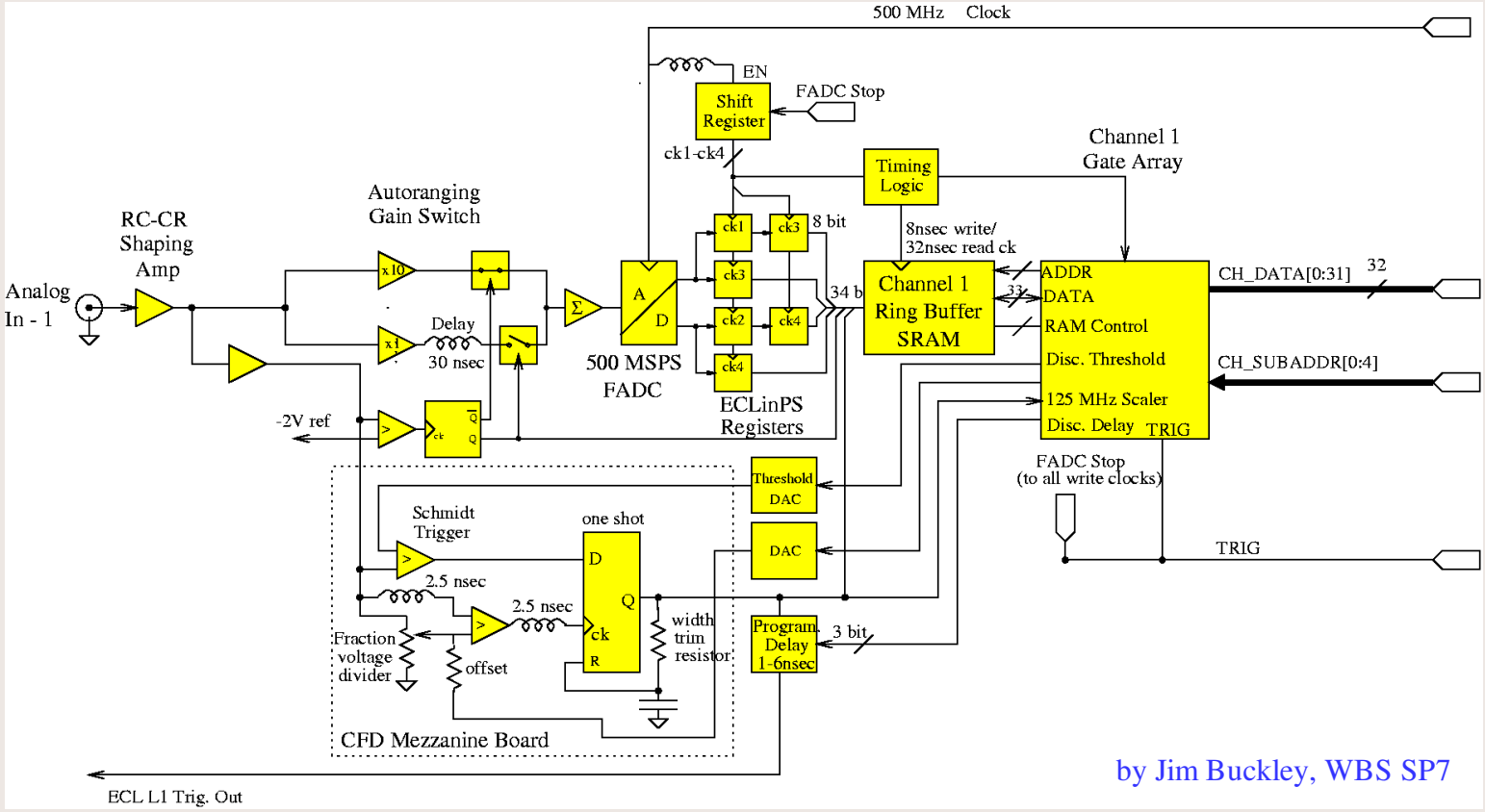
Trigger


1 pe pulse
pulse peak
rise time (10%–90%)
0.117 pe^{-1} ns^{-1}
3.5 ns
$U(t)=\frac{U_{th}}{N_{pe}}$
50 Npe
5 Npe
Npe
Amplitude
Time
[ns]
0.12
0.1
0.08
0.06
0.04
0.02
0
0 1 2 3 4 5 6 7 8 9 10

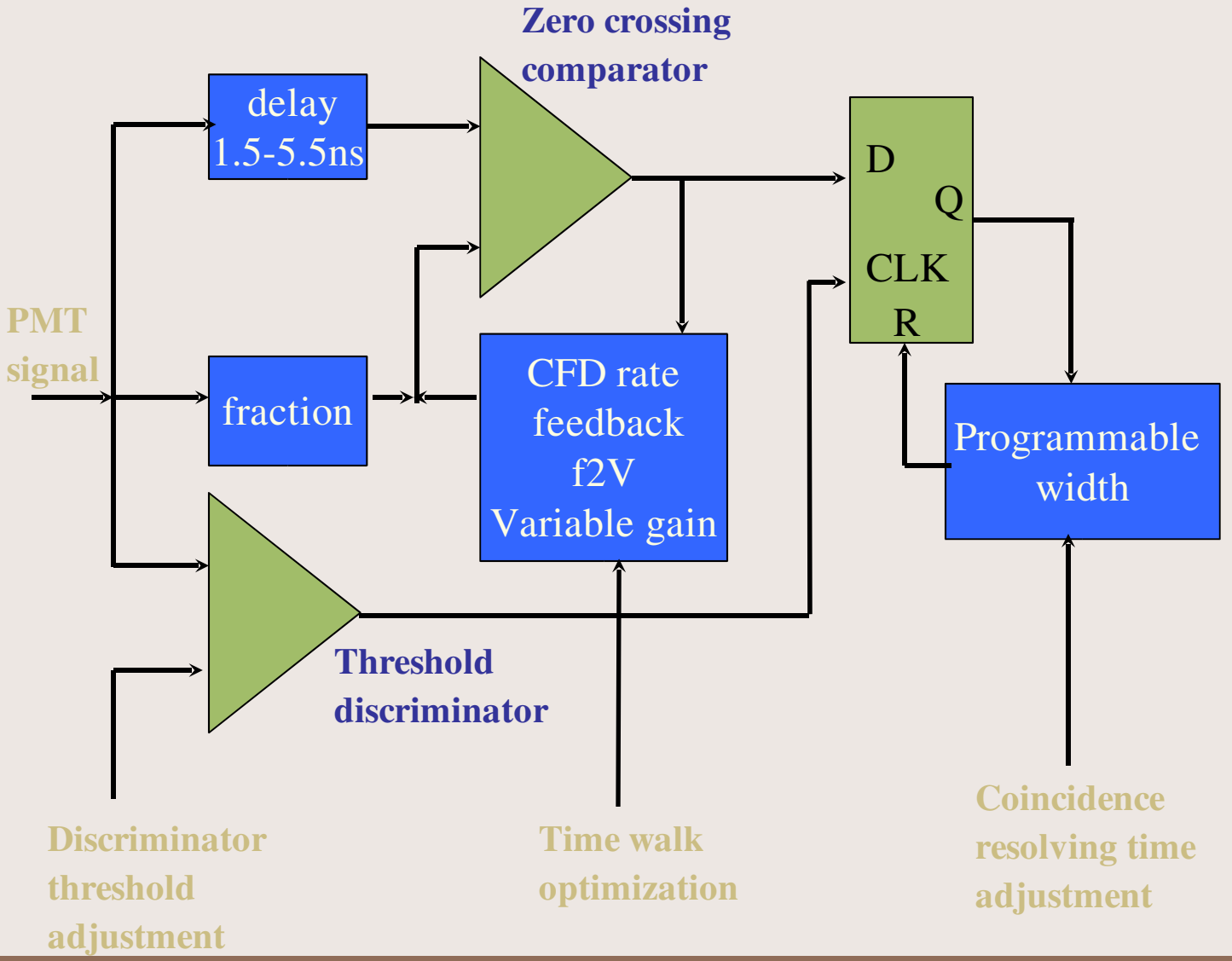
CFD in fADC channel



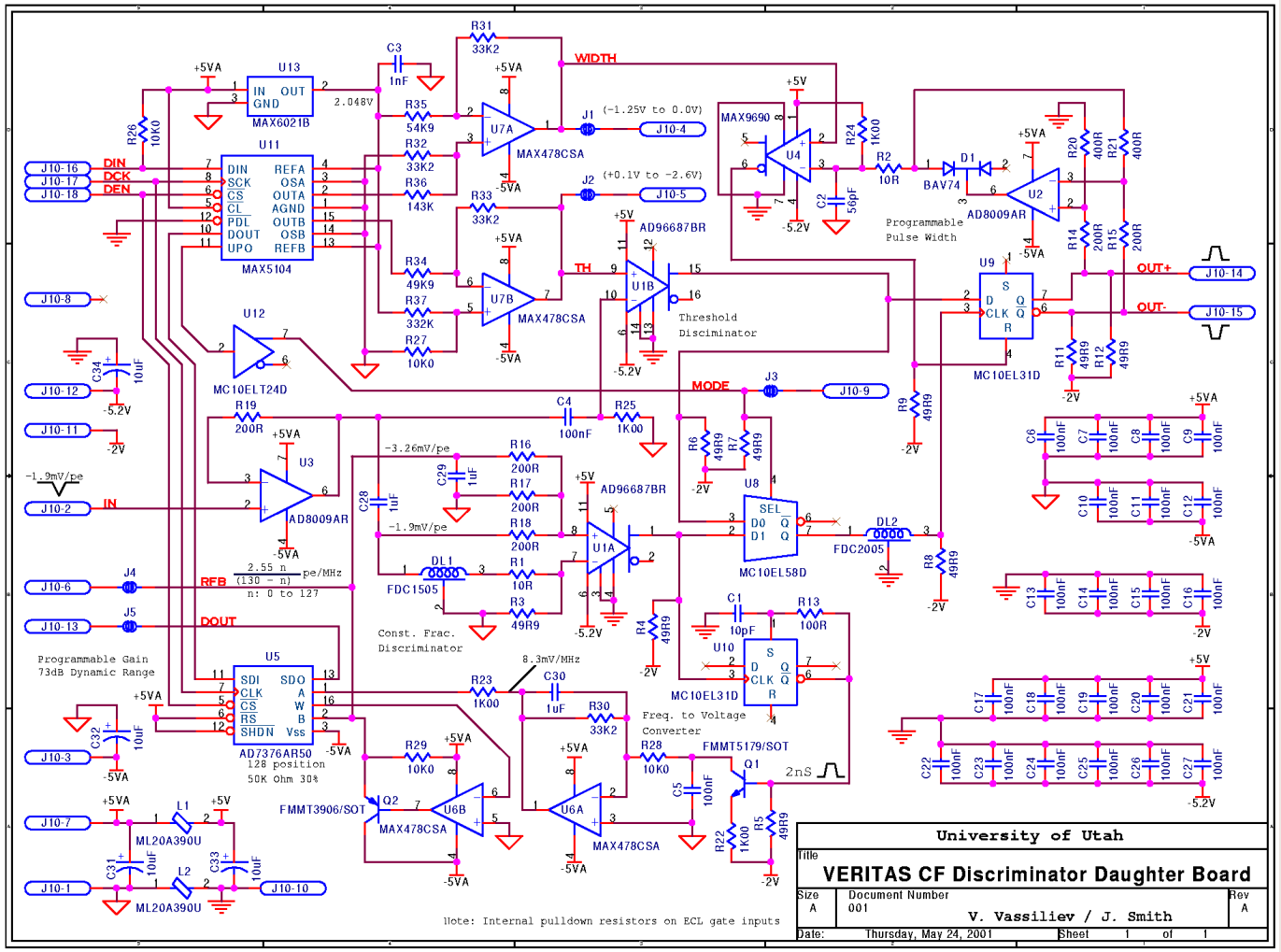
$$-(1+\frac{2}{3})\cdot N_{pe}\cdot U(t-\quad)+\frac{2}{3}\cdot N_{pe}\cdot U(t)=U_{dc}+\quad noise(t)+\sqrt{N_{pe}}\cdot\quad U(t)$$

$$-(1+\frac{2}{3})\cdot U(t-\quad)+\frac{2}{3}\cdot U(t)=\frac{U_{dc}}{N_{pe}}+\frac{noise(t)}{N_{pe}}+\sqrt{\frac{1}{N_{pe}}}\cdot\quad U(t)$$

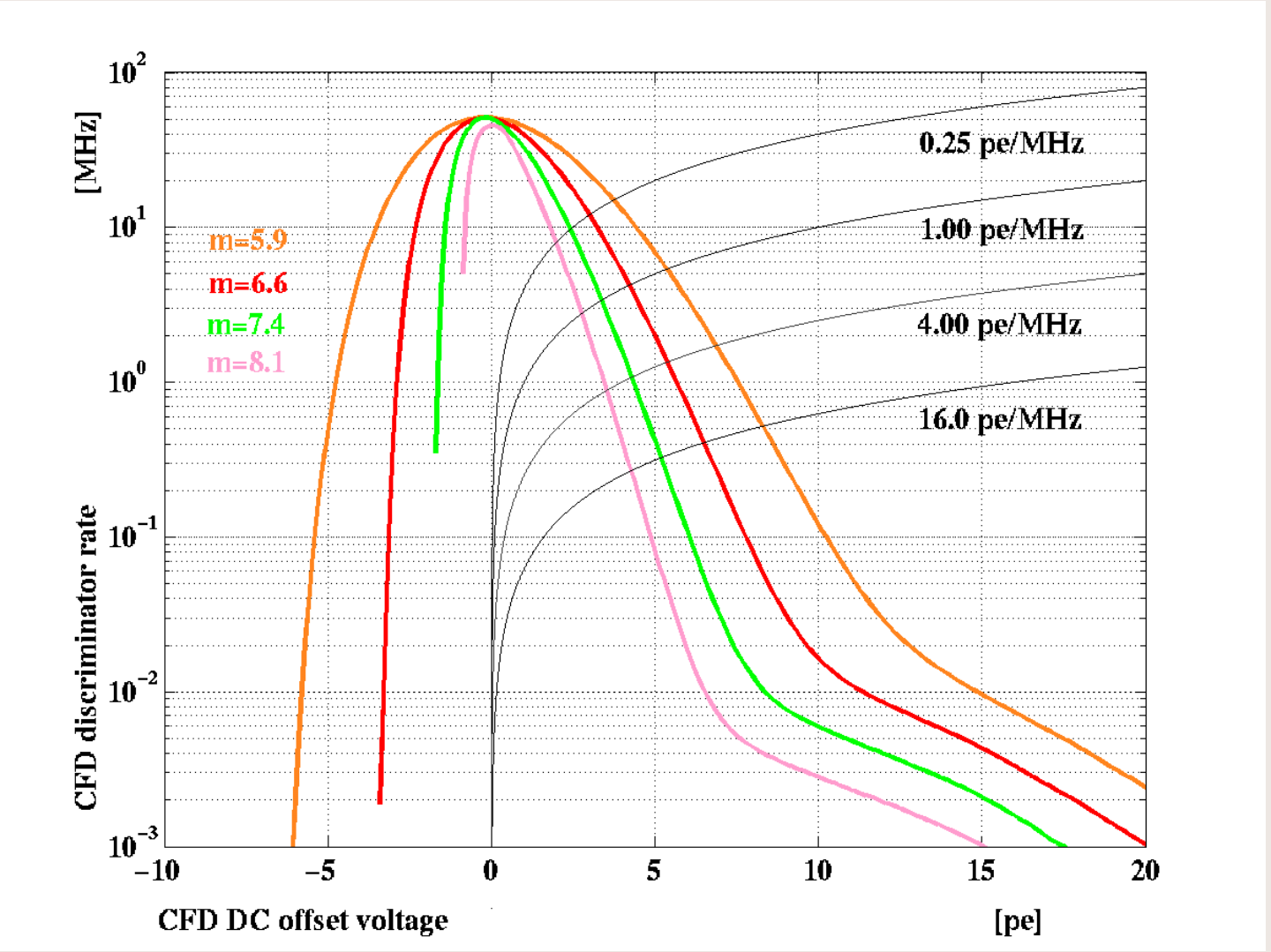
Optimization



Schematic


University of Utah
VERITAS CF Discriminator Daughter Board
V. Vassiliev / J. Smith
Thursday, May 24, 2001
Programmable Pulse Width
Threshold Discriminator
Const. Frac. Discriminator
Freq. to Voltage Converter
Programmable Gain 73dB Dynamic Range
Note: Internal pulldown resistors on ECL gate inputs
MAX6021B
MAX5104
MAX478CSA
AD96687BR
AD8009AR
MC10EL31D
MC10EL58D
MC10ELT24D
AD7376AR50
FDC1505
FDC2005
BAV74
FMMT5179/SOT
FMMT3906/SOT
ML20A390U
WIDTH
MODE
DIN
DCK
DEN
IN
RFB
DOUT
OUT+
OUT-
TH

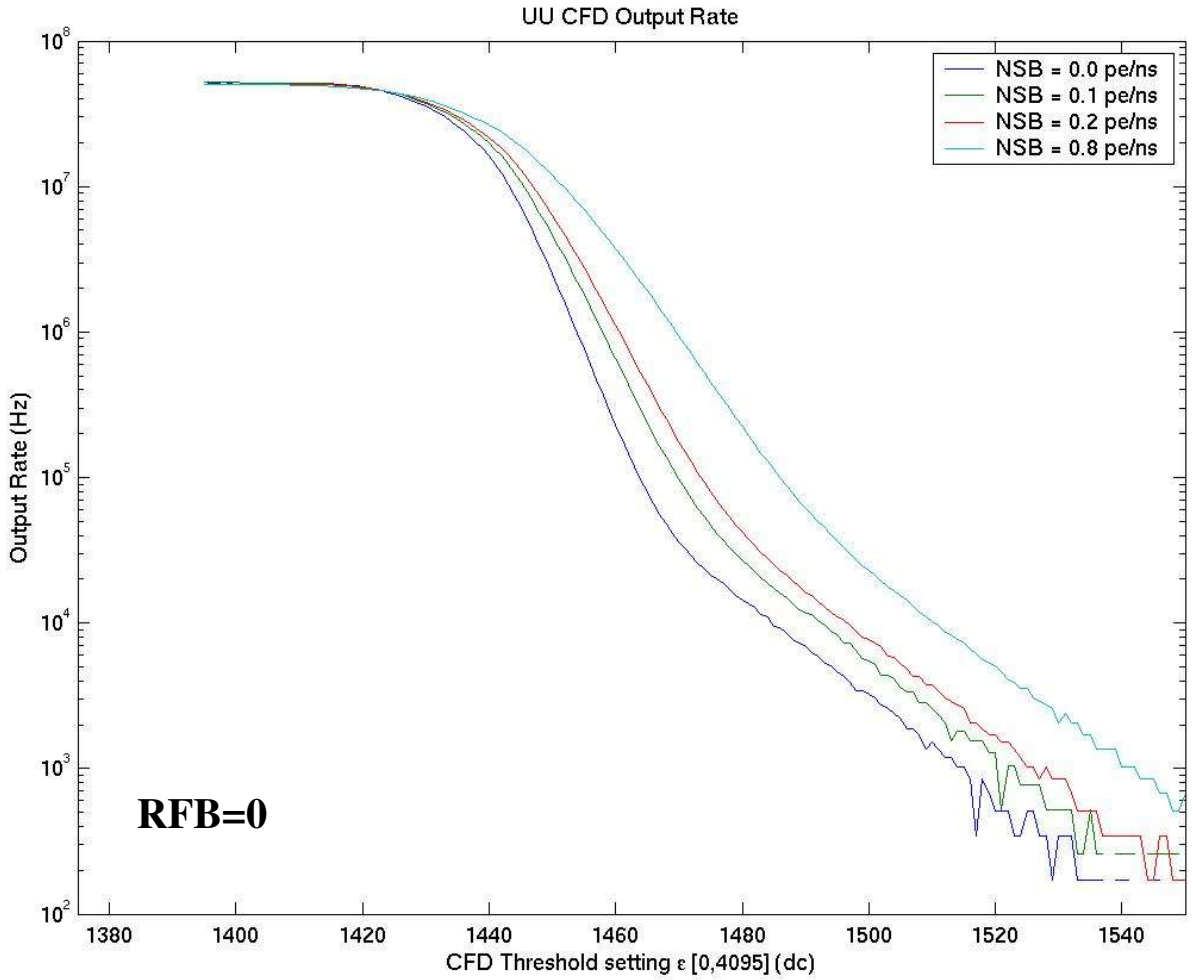
RFB


CFD discriminator rate
[MHz]
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
m=5.9
m=6.6
m=7.4
m=8.1
0.25 pe/MHz
1.00 pe/MHz
4.00 pe/MHz
16.0 pe/MHz
−10
−5
0
5
10
15
20
CFD DC offset voltage
[pe]

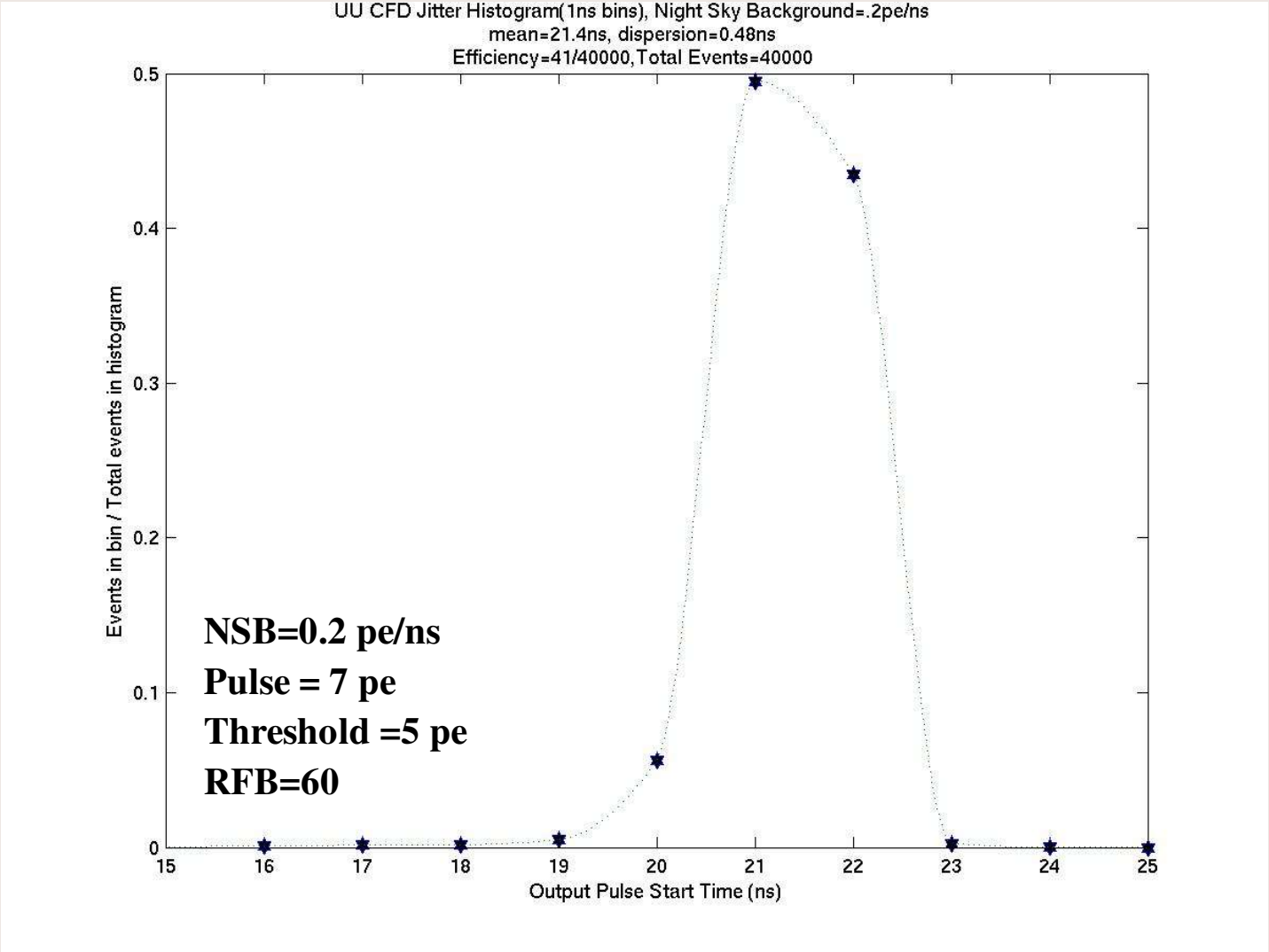
RFB benefit

- Rate compression
- Dispersion (jitter)
- Time walk (jitter)
- Efficiency

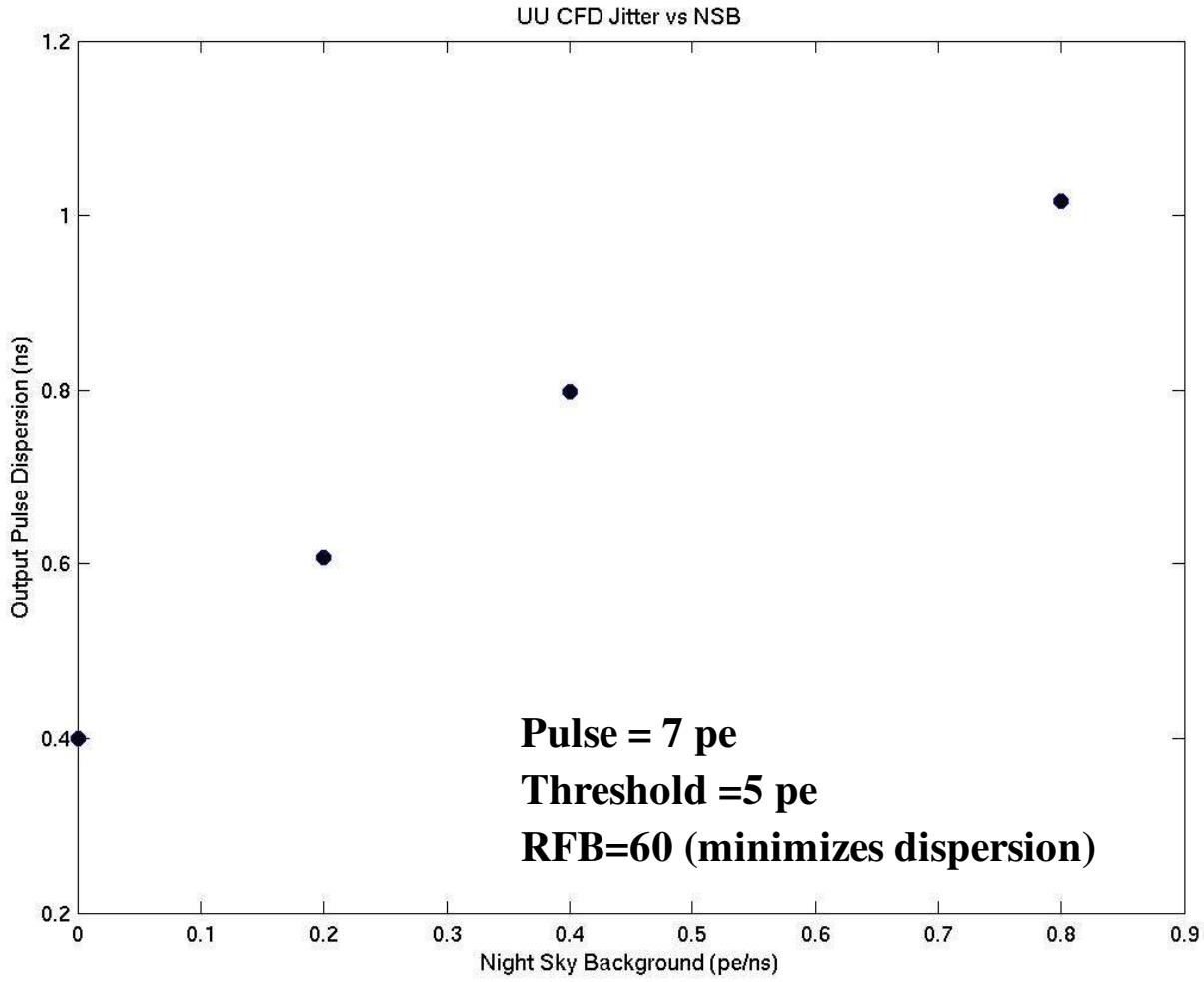
Rate vs Threshold



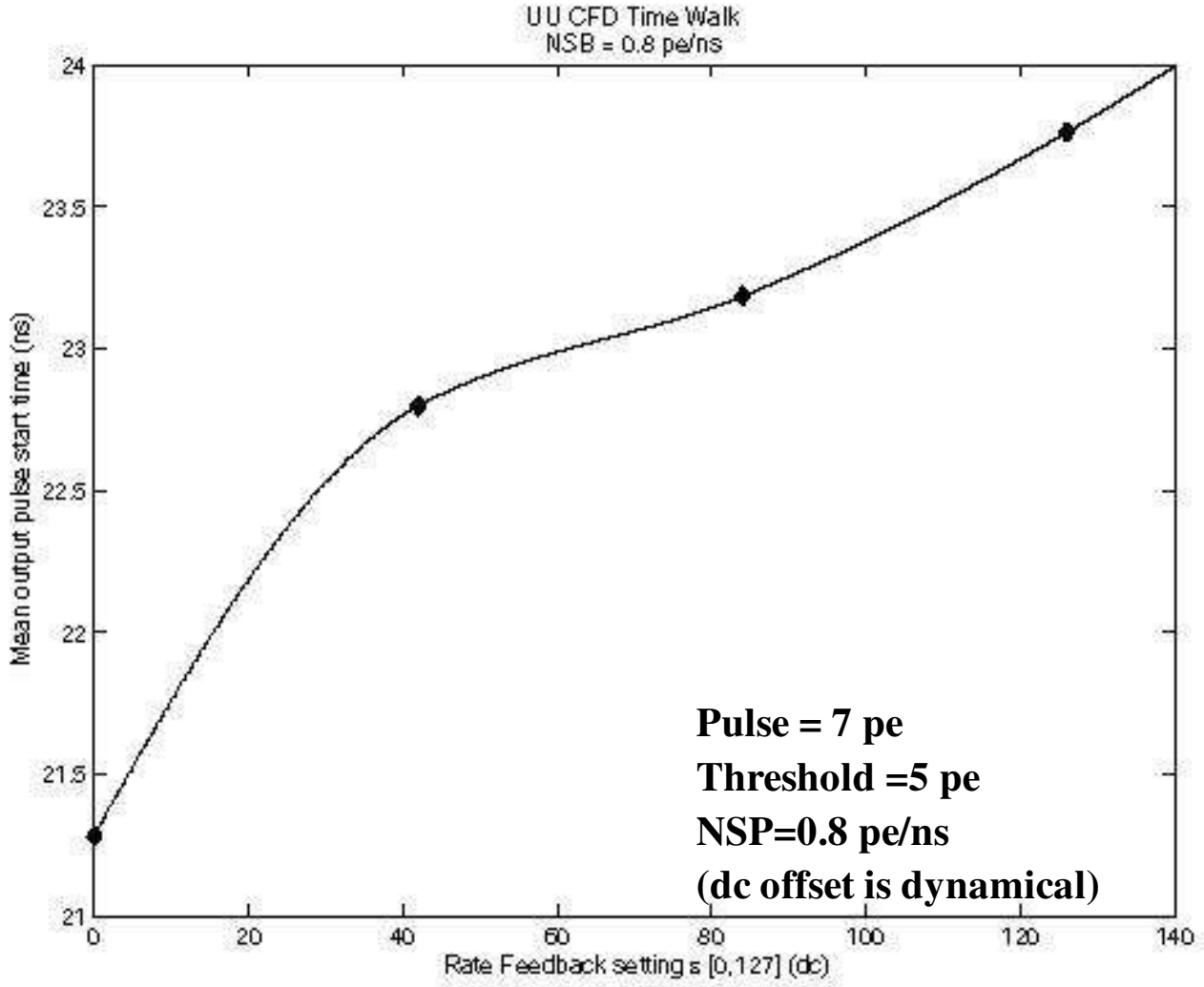
Pulse Start Time Dispersion



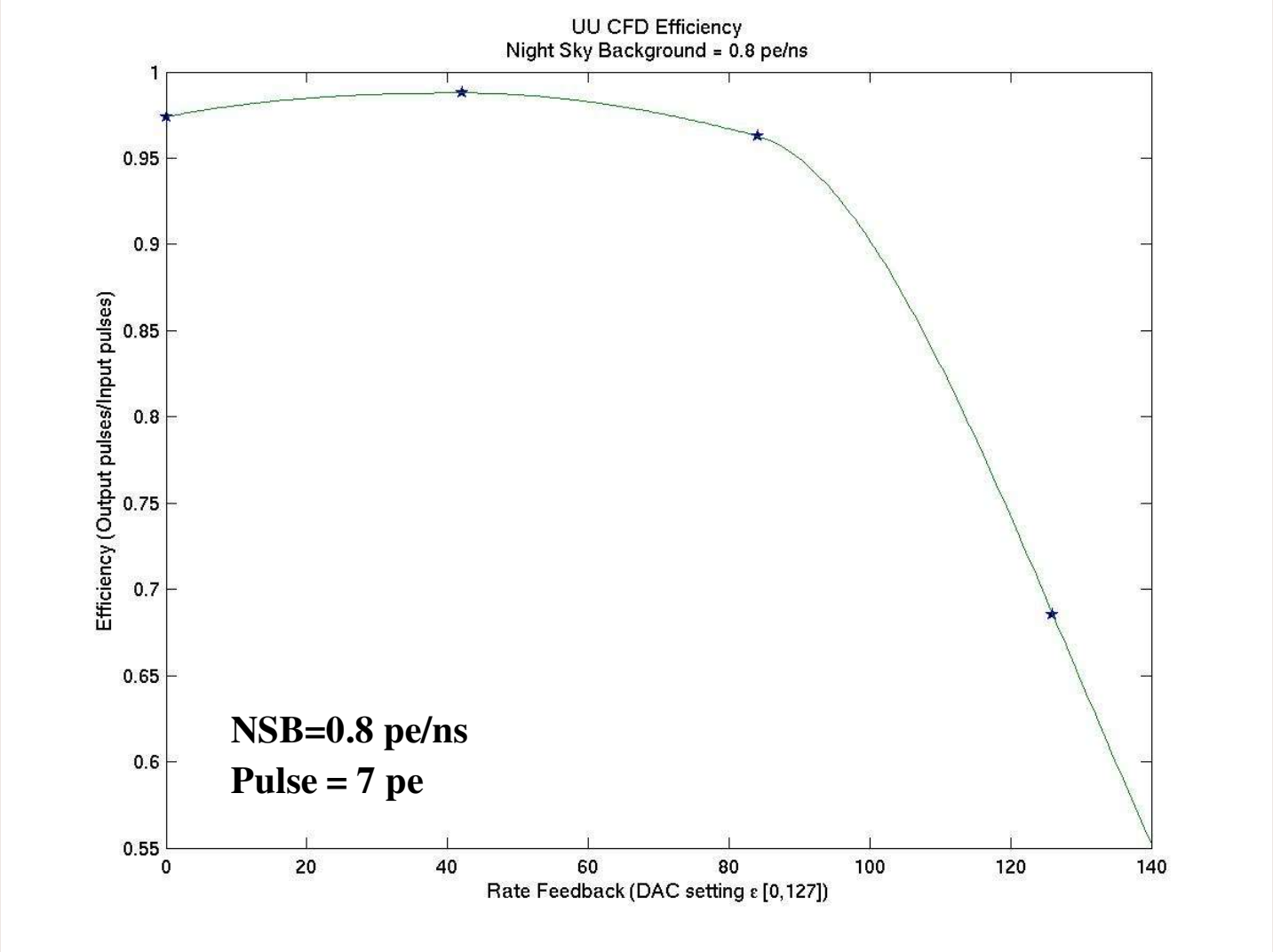
Pulse Start Time Dispersion vs NSB



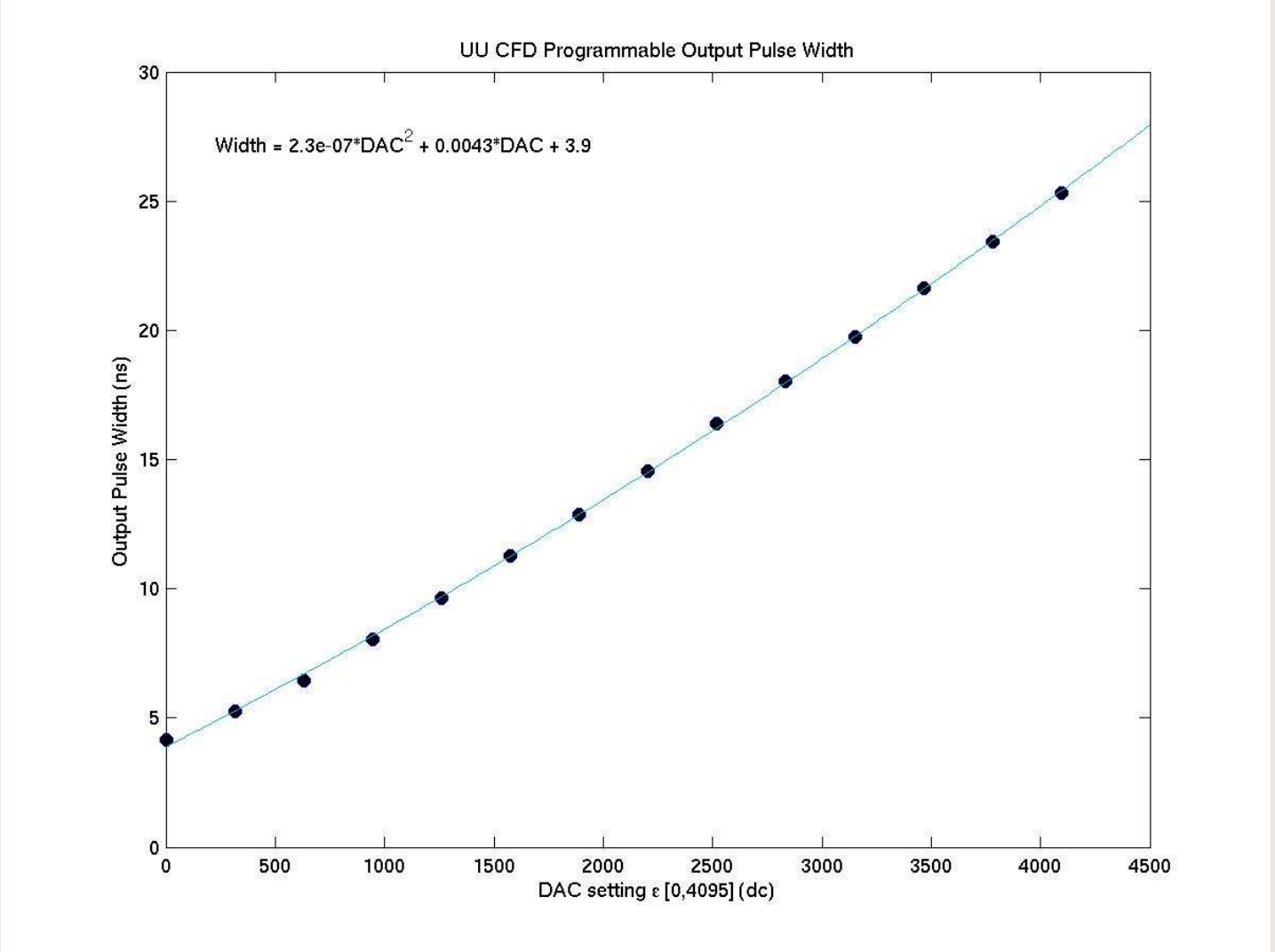
Time walk vs RFB



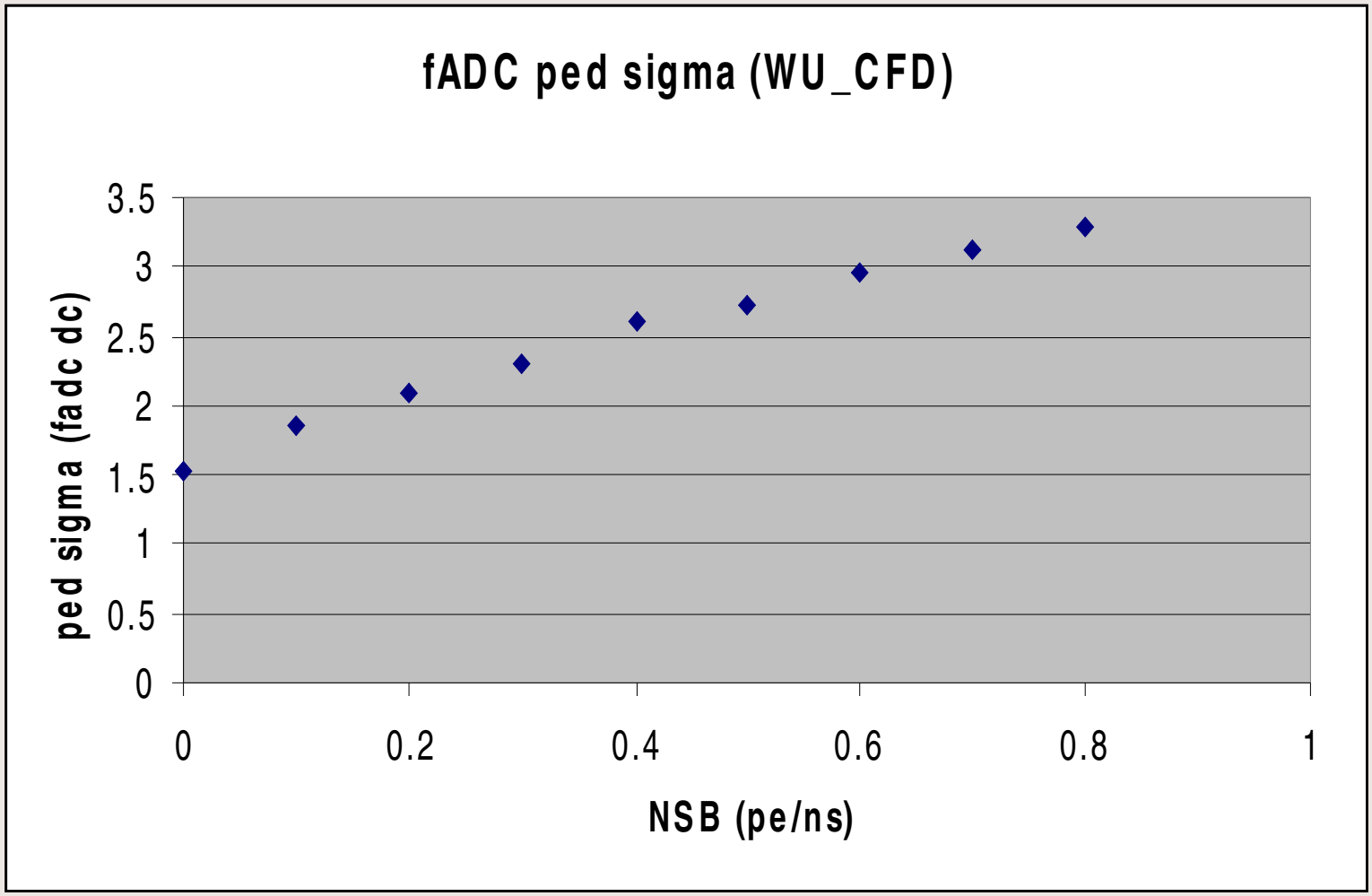
Trigger Efficiency vs RFB



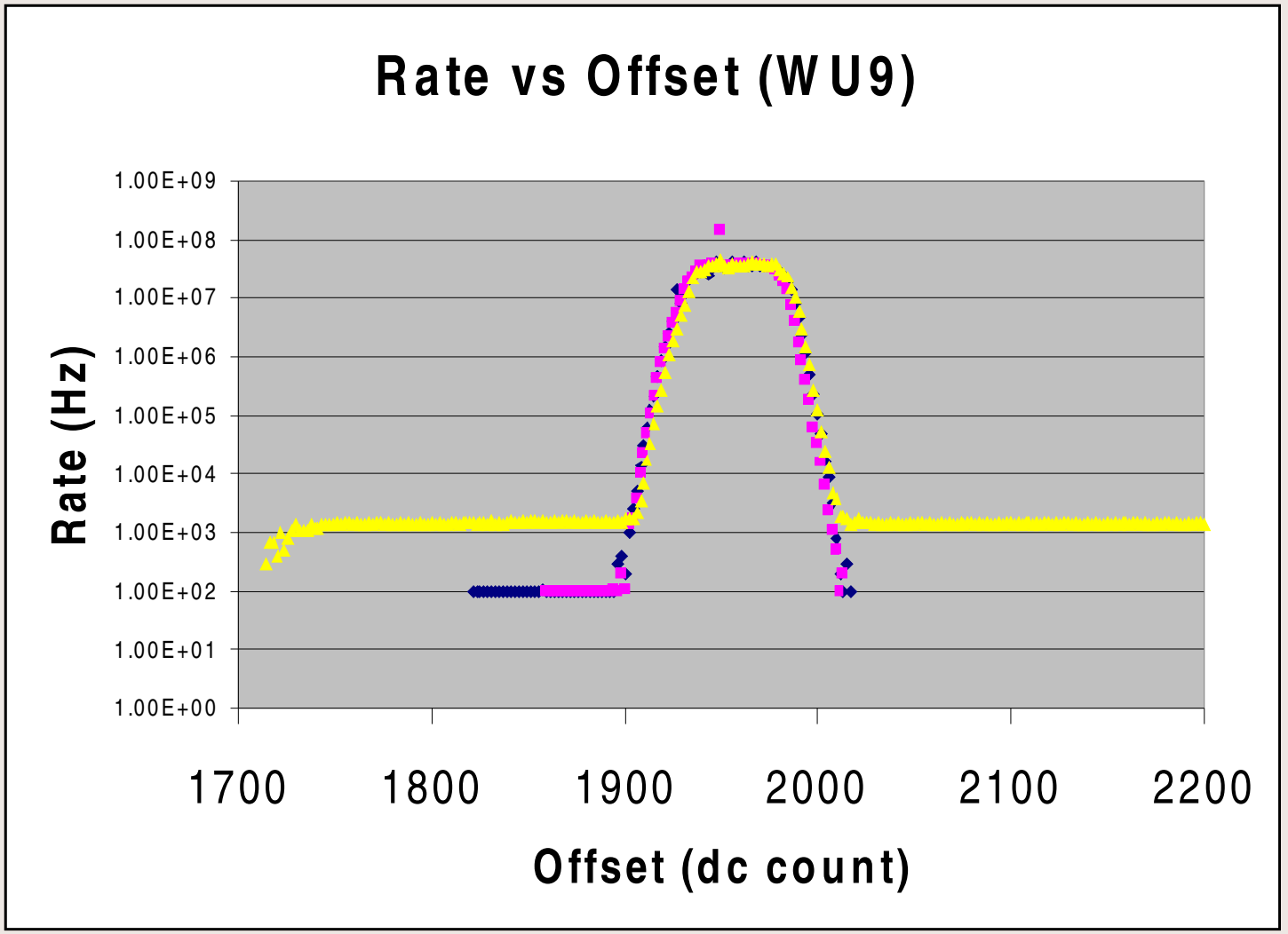
CFD output pulse width



NSB and ? noise

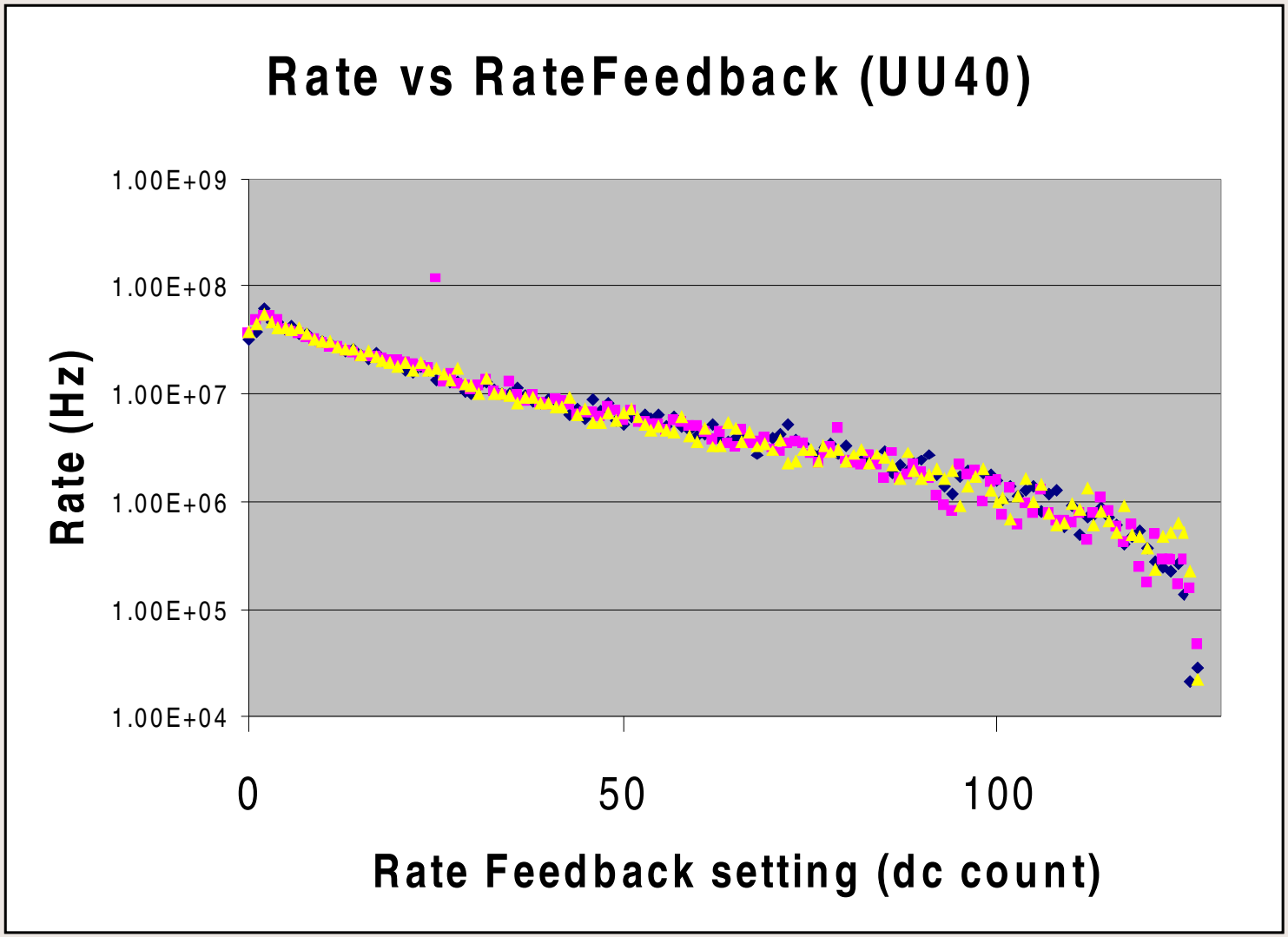


Noise in WU CFD

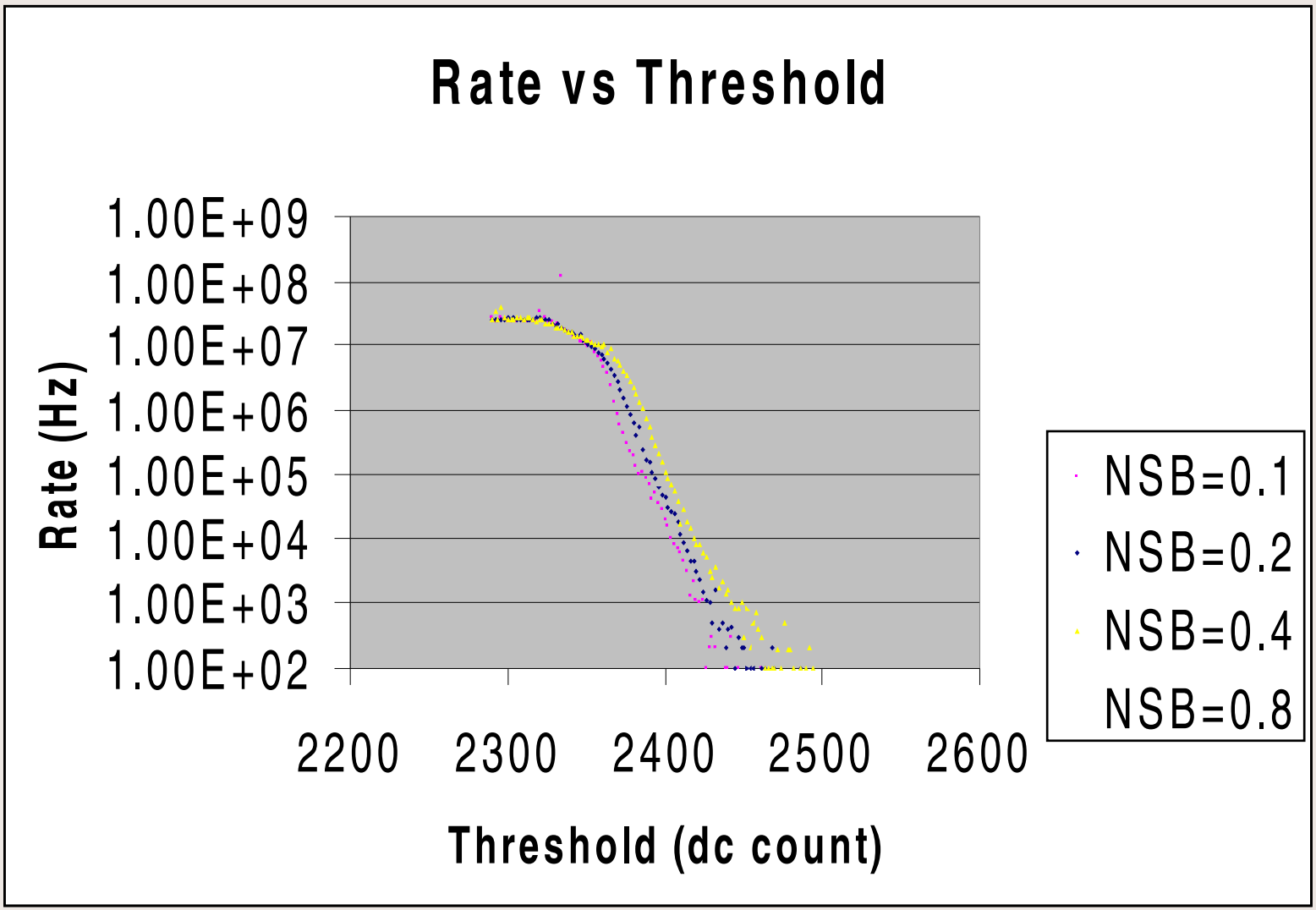


dc offset = 2440 dc (???)

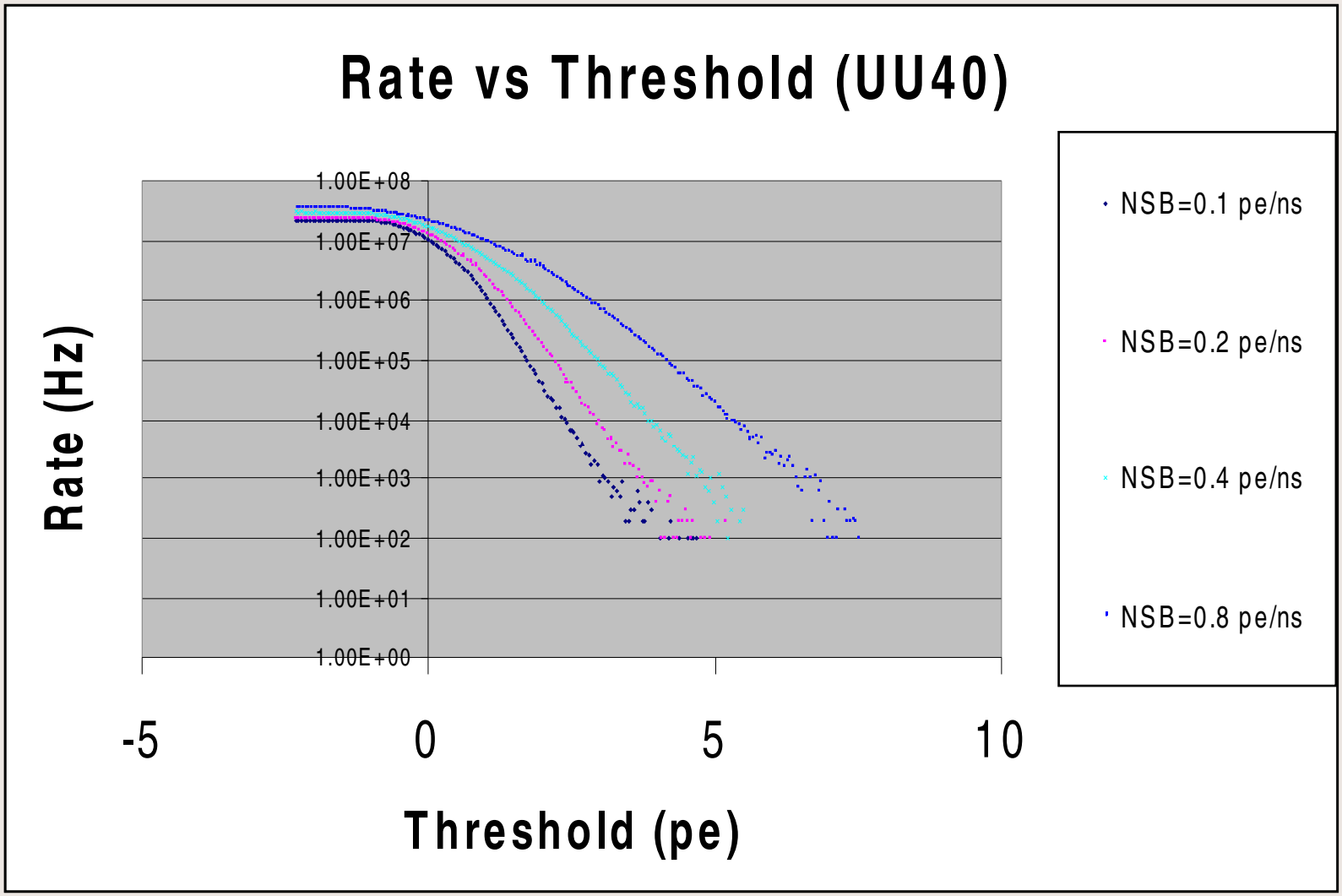
Noise in UU CFD



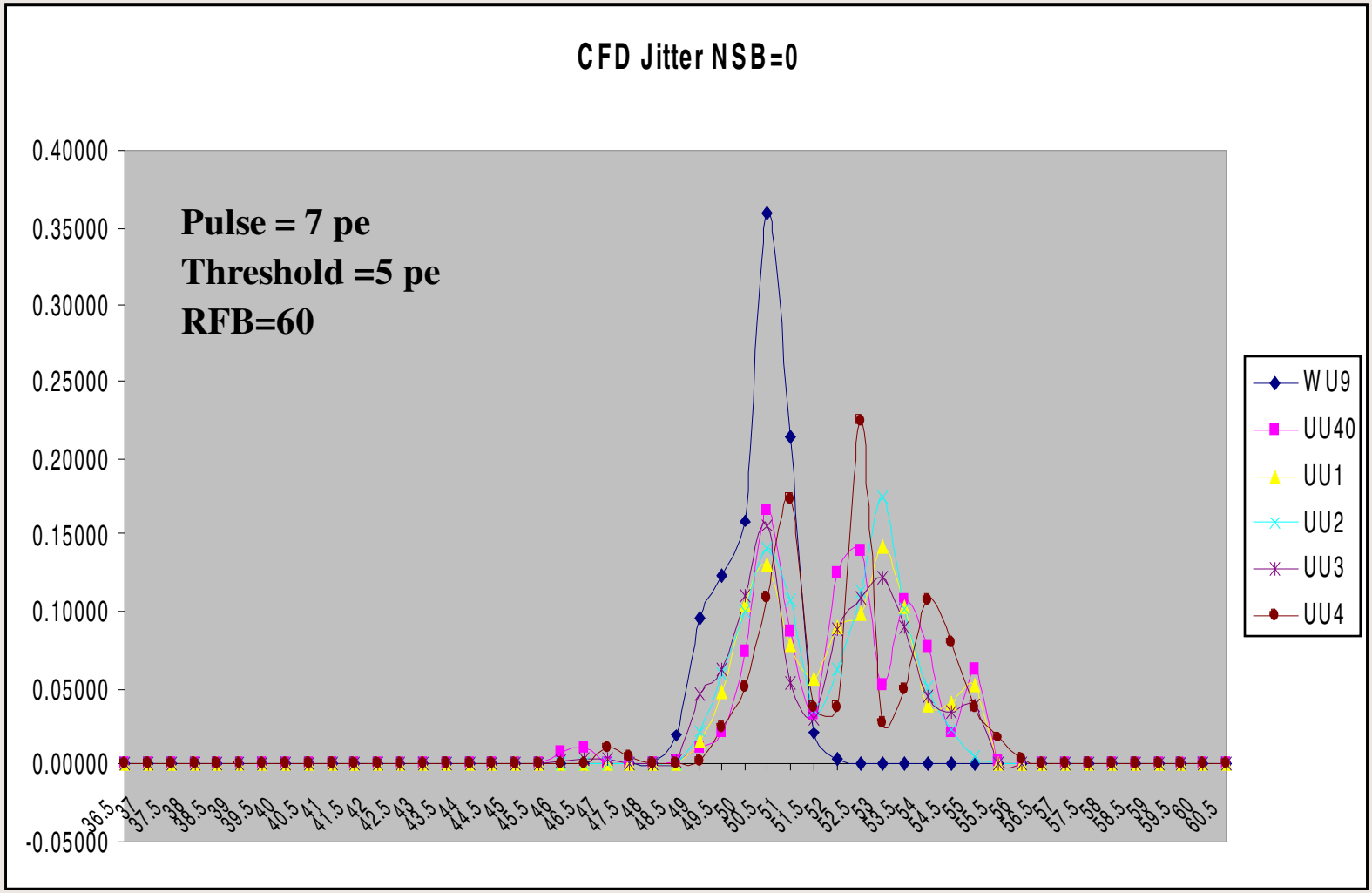
Rate vs. threshold WU9



Rate vs. threshold UU40

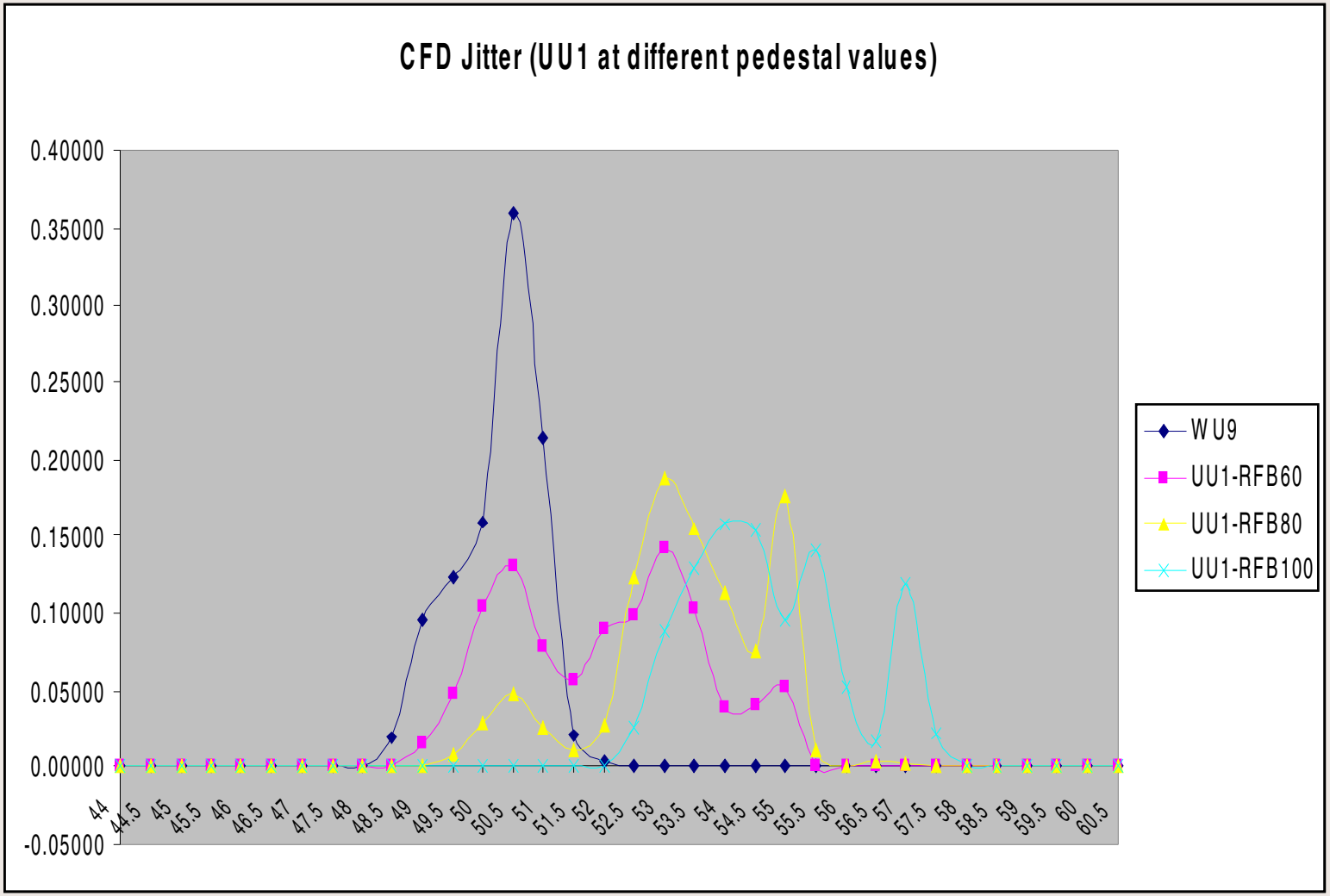


Jitter (on fADC board)

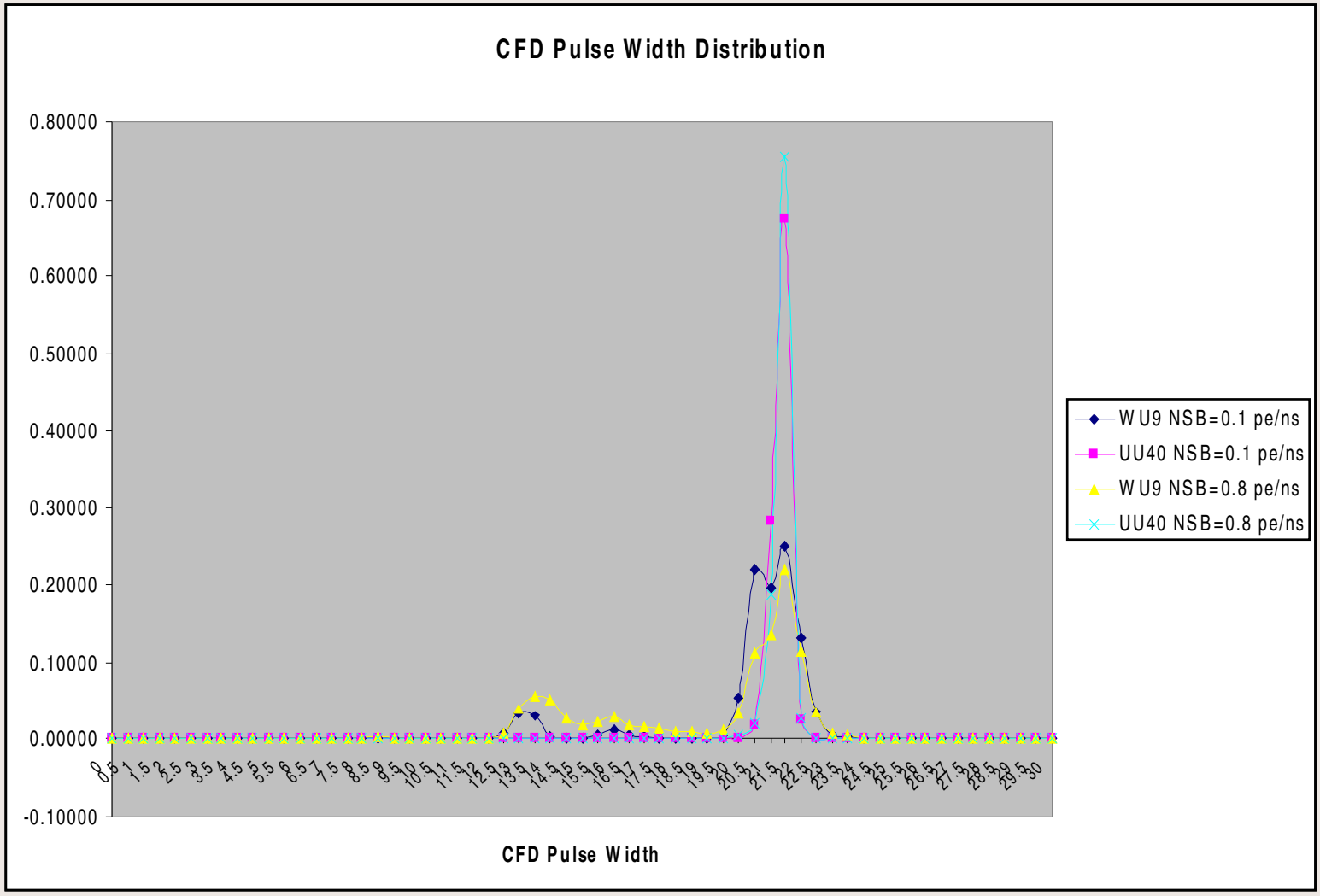


Sigma WU=0.73 ns; **Sigma UU=1.33-1.73 ns**

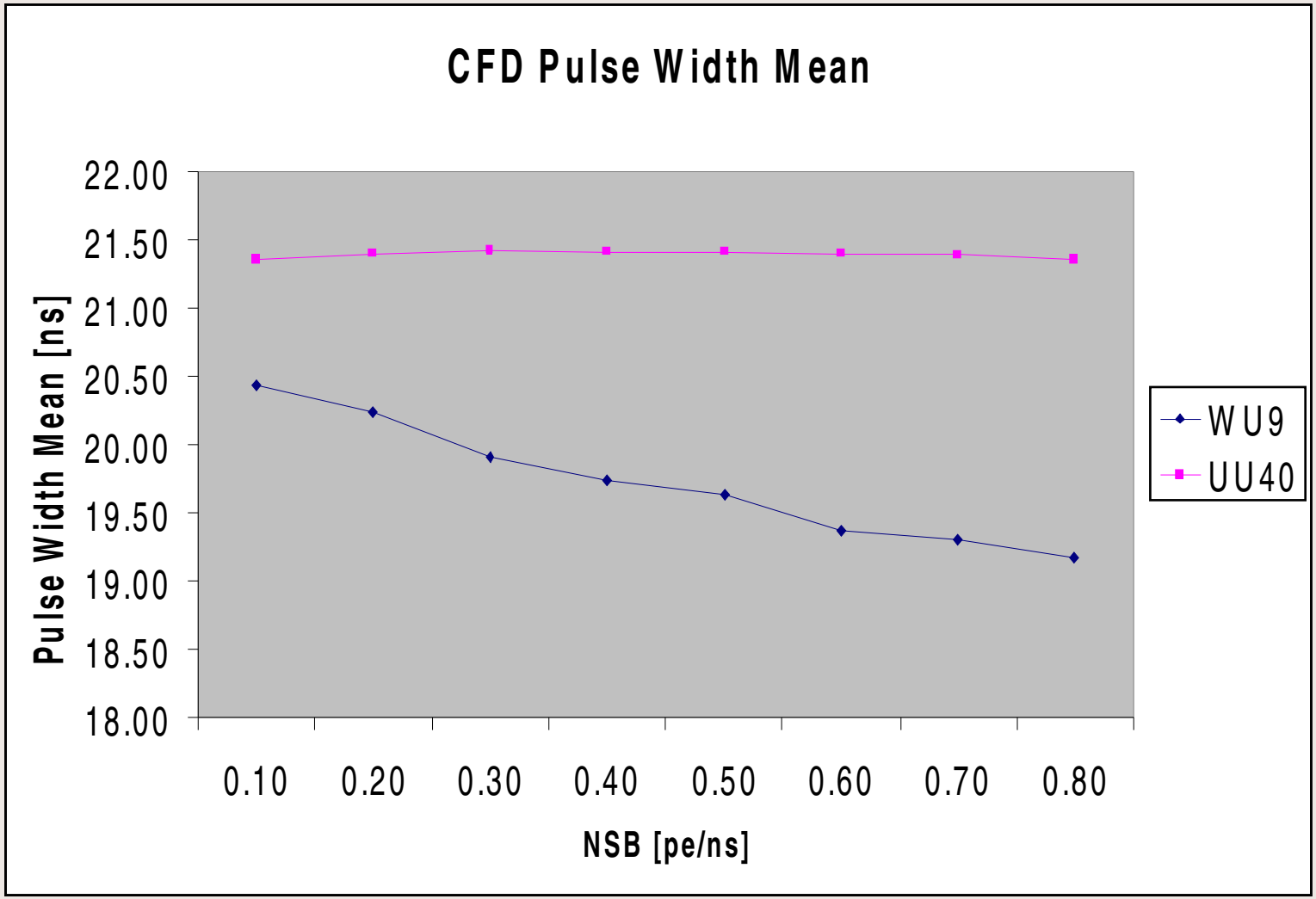
“WU-like”


CFD Jitter (UU1 at different pedestal values)
0.40000
0.35000
0.30000
0.25000
0.20000
0.15000
0.10000
0.05000
0.00000
-0.05000
44
44.5
45
45.5
46
46.5
47
47.5
48
48.5
49
49.5
50
50.5
51
51.5
52
52.5
53
53.5
54
54.5
55
55.5
56
56.5
57
57.5
58
58.5
59
59.5
60
60.5
WU9
UU1-RFB60
UU1-RFB80
UU1-RFB100

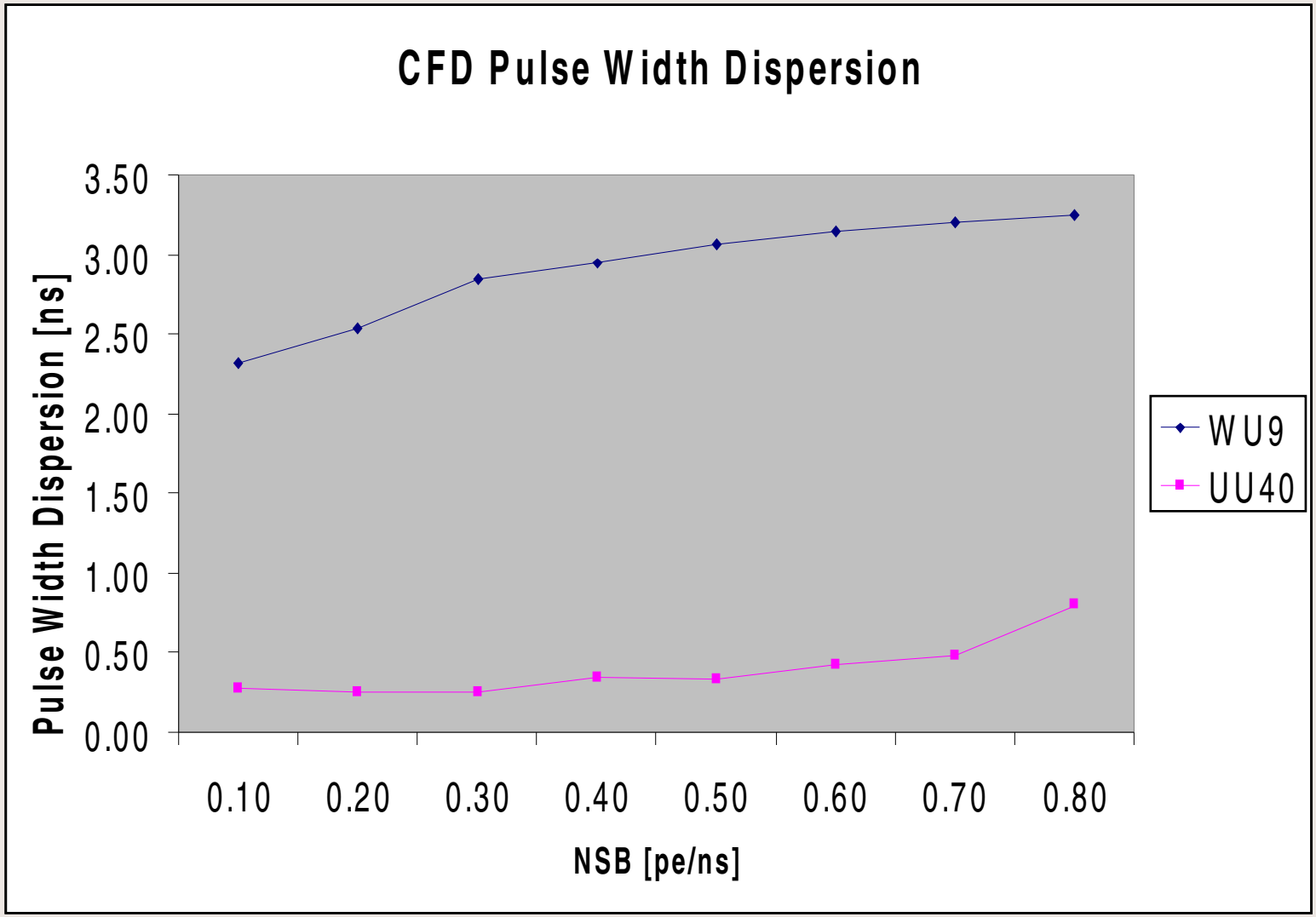
CFD pulse Width



Mean time change



CFD pulse width dispersion



UU_CFD vs. WU_CFD

- CFD output pulse width is programmable
- CFD output pulse width stability
- Fraction vs. delay lines optimized (no 2nd DL)
- DC offset -> RFB (demonstrated in the lab)

- Noise problem (500 MHz ?)
- Jitter has increased (on fADC board)
- RFB malfunctions since NSB < ? noise

Plans ?

- Layout review -when ?, cost?
- Layout change (fADC, CFD, CFD test board)

  when will we know about this ?

  who makes the decision?
- Gain increase ?

  will this work (test on fADC)
- fcasfc

Options